Fig. 1

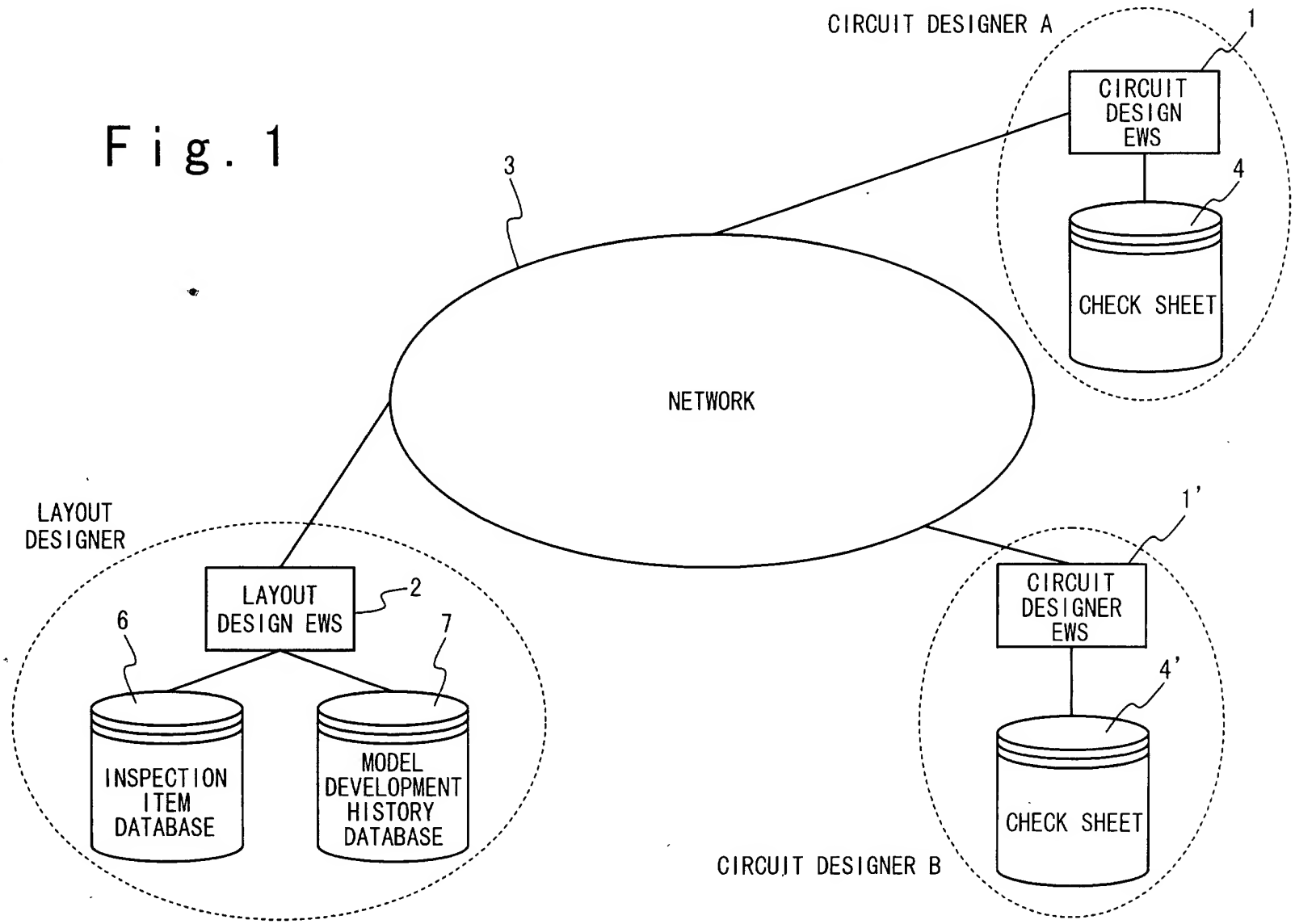

CIRCUIT DESIGNER A
1
CIRCUIT DESIGN EWS
4
CHECK SHEET
3
NETWORK
LAYOUT DESIGNER
LAYOUT DESIGN EWS
2
6
7
INSPECTION ITEM DATABASE
MODEL DEVELOPMENT HISTORY DATABASE
1'
CIRCUIT DESIGNER EWS
4'
CHECK SHEET
CIRCUIT DESIGNER B

Fig. 2

4:CHECK SHEET

CIRCUIT FEATURE								INSPECTION ITEM AND RESULT			
TECHNOLOGY	CONDITION	MODEL NAME	PACKAGE	THE NUMBER OF PINS	SCAN	BOUNDARY SCAN	RAM	NET LIST CHECK	PATTERN CHECK	SCAN CHECK	TIMING CHECK
CMOS9HD	cmos_3.3V	65956E00	TBG	420	USED	NOT-USED	NOT-USED	ERROR 0	ERROR 2	NOT-EXECUTED	ERROR 0

EPSON 0.5-34 EPSON

Fig. 3

6: INSPECTION ITEM DATABASE

CIRCUIT FEATURE	INSPECTION ITEM						
	NET LIST CHECK	PATTERN CHECK	SCAN CHECK	BOUNDARY SCAN CHECK	TIMING CHECK	TEST TERMINAL CHECK	RAM CHECK
BASIC CONFIGURATION	EXECUTED	EXECUTED			EXECUTED		
USAGE OF THE SCAN	EXECUTED	EXECUTED	EXECUTED		EXECUTED		
USAGE OF THE BOUNDARY SCAN	EXECUTED	EXECUTED		EXECUTED	EXECUTED		
USAGE OF THE RAM	EXECUTED	EXECUTED			EXECUTED		EXECUTED
TEST BUS CONFIGURATION	EXECUTED	EXECUTED			EXECUTED	EXECUTED	
...	...	...	...	...	...	...	...

Fig. 4

7:MODEL DEVELOPMENT HISTORY DATABASE

IDINFORMATION	CIRCUIT FEATURE				:	INSPECTION ITEM ECXECUTION HISTORY							
	TECHNOLOGY	CONDITION	MODEL NAME	PACKAGE	:	PHASE	DATA	NET LIST CHECK	PATTERN CHECK	SCAN CHECK	BOUNDARY SCANCHECK	TIMING CHECK	:
AAA	CMOS9HD	cmos_3.3V	6595 6E00	TBG	:	ACCEPTED	9/11	ERROR 0	ERROR 2	NOT-EXECUTED	NOT-TARGETED	ERROR 0	:
						RE-ACCEPTED	9/14	ERROR 0	ERROR 0	ERROR 0	NOT-TARGETED	ERROR 0	:
						BACK ANNOTATION	9/18	ERROR 0	ERROR 0	ERROR 0	NOT-TARGETED	ERROR 0	:
	CB7	ttl_5V	87543	QOGN	:	ACCEPTED	9/4	EXCEPTED	ERROR 0	NOT-TARGETED	ERROR 0	ERROR 0	:
						BACK ANNOTATION	9/11	ERROR 0	ERROR 0	NOT-TARGETED	ERROR 0	ERROR 0	:
ABC	CB8	ttl_3.3V	12345	A8SI	:	ACCEPTED	8/3	ERROR 0	ERROR 0	ERROR 0	NOT-TARGETED	ERROR 0	:
						BACK ANNOTATION	8/7	ERROR 0	ERROR 0	ERROR 0	NOT-TARGETED	ERROR 0	:
	CMOS6	cmos_5V	6562 4E99	QFP	:	ACCEPTED	7/29	ERROR 0	ERROR 0	NOT-TARGETED	NOT-TARGETED	ERROR 0	:
						BACK ANNOTATION	9/4	ERROR 0	ERROR 0	NOT-TARGETED	NOT-TARGETED	ERROR 0	:
	:	:	:	:		:	:	:	:	:	:	:	

Fig. 5

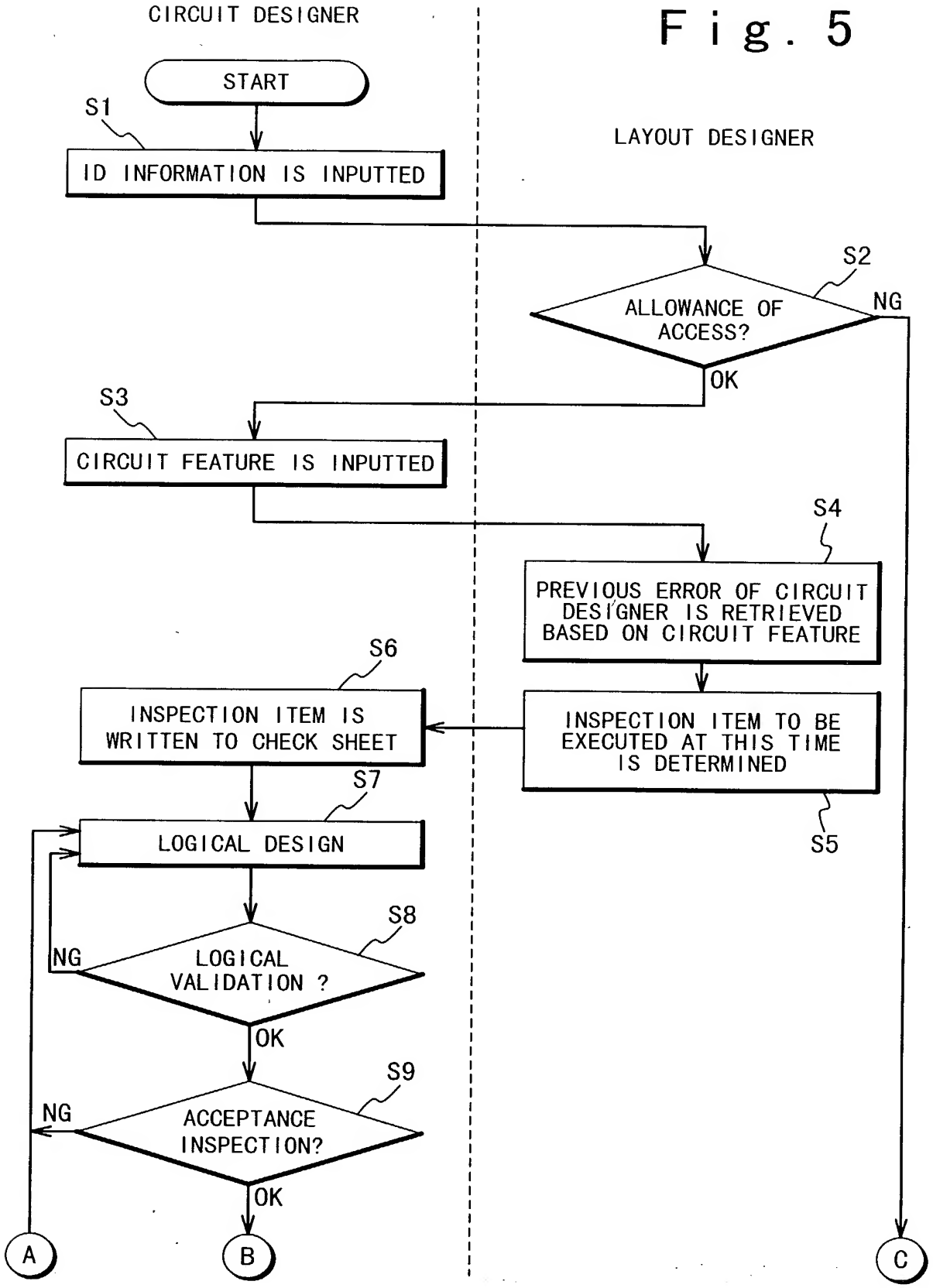

CIRCUIT DESIGNER
LAYOUT DESIGNER
START
S1
ID INFORMATION IS INPUTTED
S2
ALLOWANCE OF ACCESS?
NG
OK
S3
CIRCUIT FEATURE IS INPUTTED
S4
PREVIOUS ERROR OF CIRCUIT DESIGNER IS RETRIEVED BASED ON CIRCUIT FEATURE
INSPECTION ITEM TO BE EXECUTED AT THIS TIME IS DETERMINED
S5
S6
INSPECTION ITEM IS WRITTEN TO CHECK SHEET
S7
LOGICAL DESIGN
S8
LOGICAL VALIDATION ?
NG
OK
S9
ACCEPTANCE INSPECTION?
NG
OK
A
B
C

Fig. 6

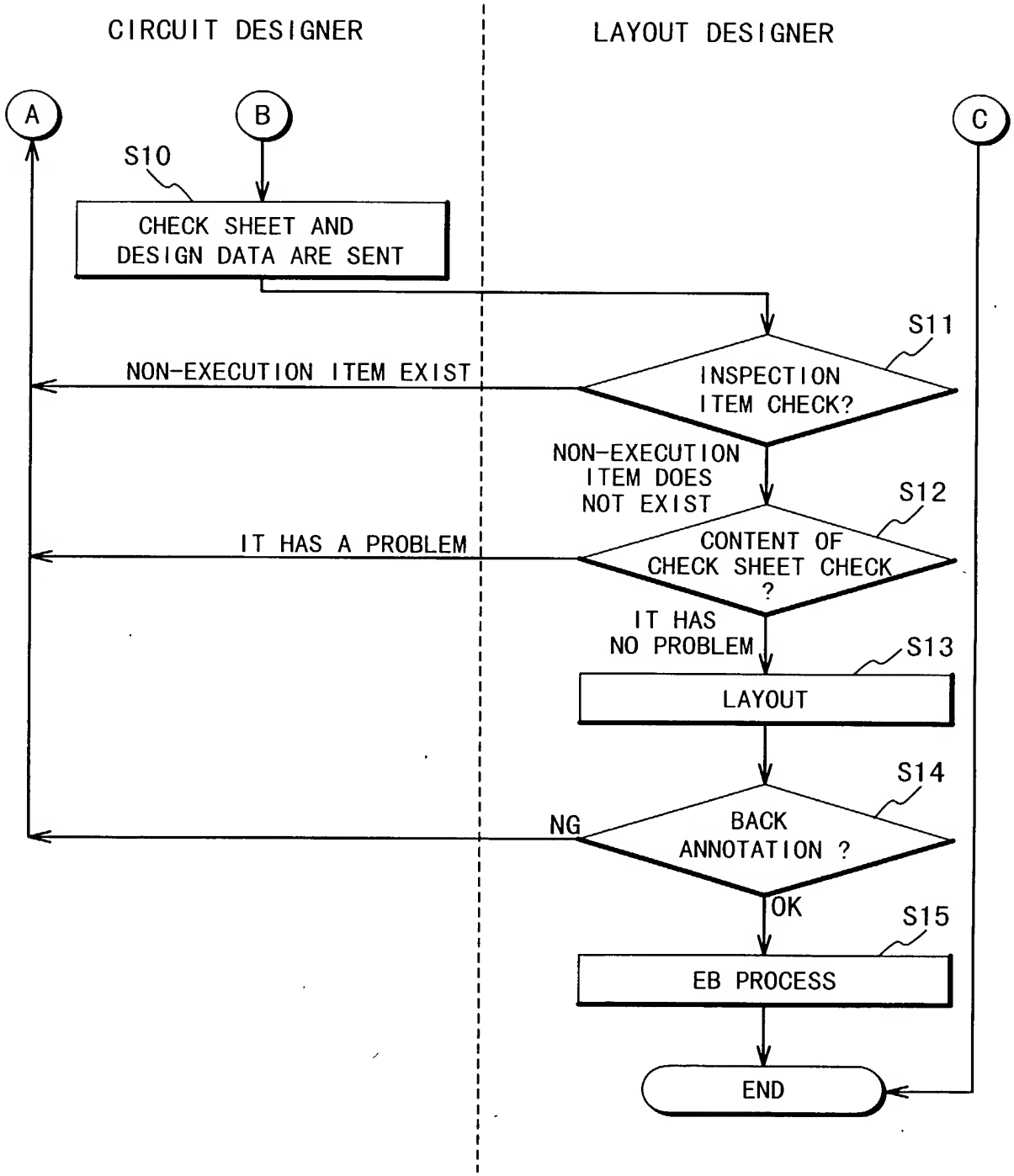

CIRCUIT DESIGNER
LAYOUT DESIGNER
A
B
C
S10
CHECK SHEET AND DESIGN DATA ARE SENT
S11
INSPECTION ITEM CHECK?
NON-EXECUTION ITEM EXIST
NON-EXECUTION ITEM DOES NOT EXIST
S12
CONTENT OF CHECK SHEET CHECK ?
IT HAS A PROBLEM
IT HAS NO PROBLEM
S13
LAYOUT
S14
BACK ANNOTATION ?
NG
OK
S15
EB PROCESS
END

Fig. 7

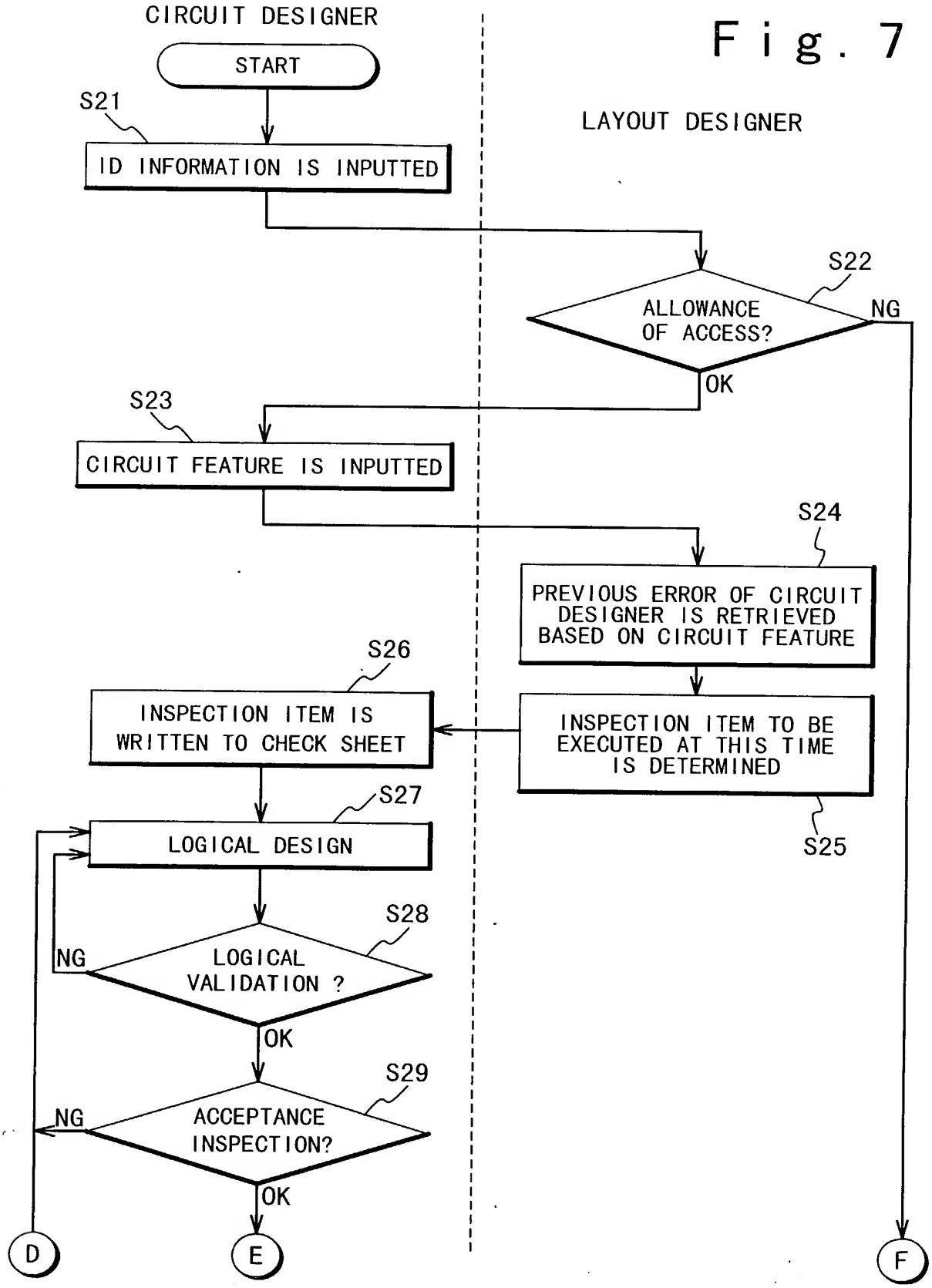

CIRCUIT DESIGNER
LAYOUT DESIGNER
START
S21
ID INFORMATION IS INPUTTED
S22
ALLOWANCE OF ACCESS?
NG
OK
S23
CIRCUIT FEATURE IS INPUTTED
S24
PREVIOUS ERROR OF CIRCUIT DESIGNER IS RETRIEVED BASED ON CIRCUIT FEATURE
INSPECTION ITEM TO BE EXECUTED AT THIS TIME IS DETERMINED
S25
S26
INSPECTION ITEM IS WRITTEN TO CHECK SHEET
S27
LOGICAL DESIGN
S28
LOGICAL VALIDATION ?
NG
OK
S29
ACCEPTANCE INSPECTION?
NG
OK
D
E
F

Fig. 8

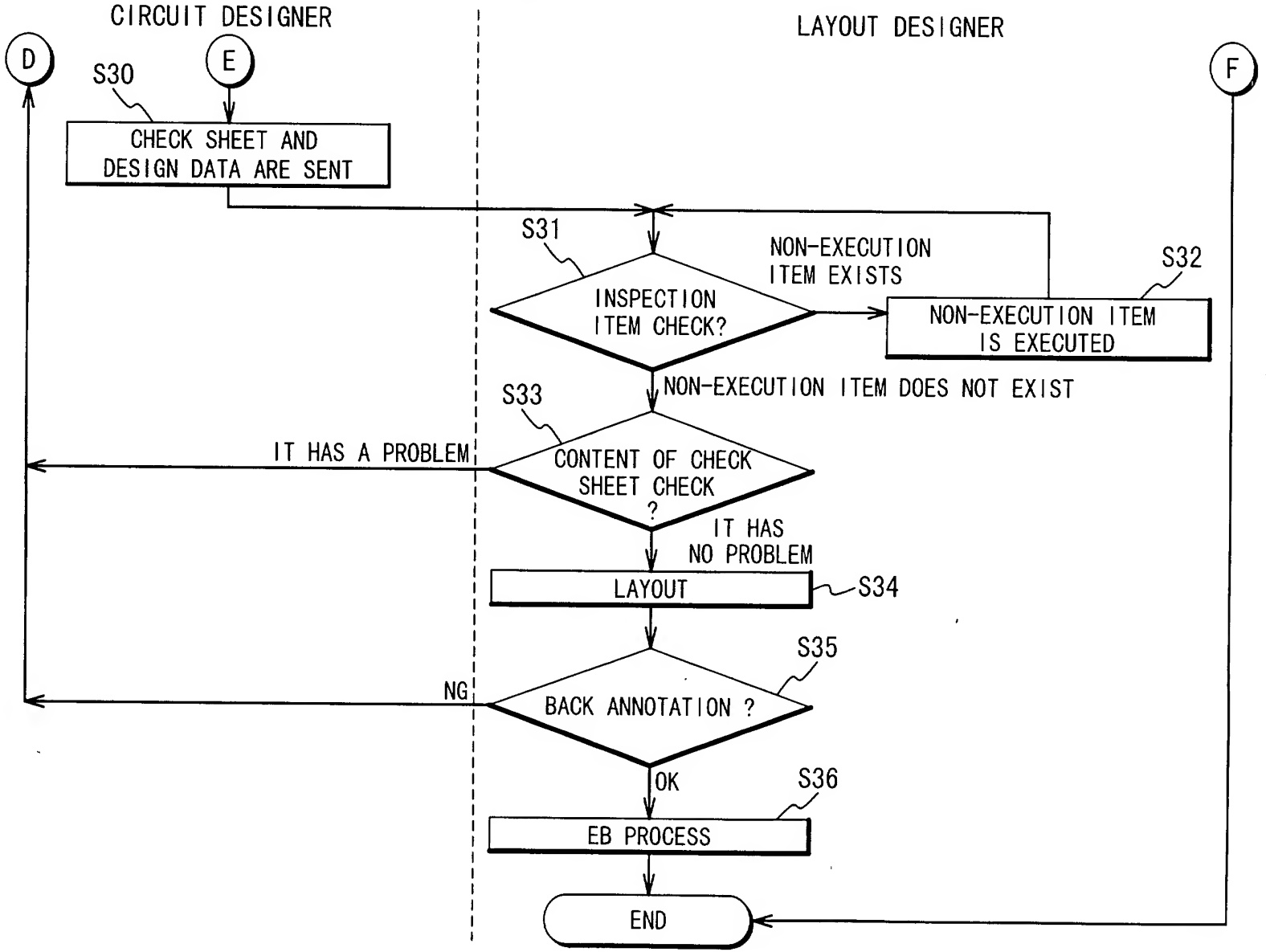

CIRCUIT DESIGNER
LAYOUT DESIGNER
D
E
F
S30
CHECK SHEET AND DESIGN DATA ARE SENT
S31
INSPECTION ITEM CHECK?
NON-EXECUTION ITEM EXISTS
S32
NON-EXECUTION ITEM IS EXECUTED
NON-EXECUTION ITEM DOES NOT EXIST
S33
CONTENT OF CHECK SHEET CHECK ?
IT HAS A PROBLEM
IT HAS NO PROBLEM
LAYOUT
S34
S35
BACK ANNOTATION ?
NG
OK
S36
EB PROCESS
END

Fig. 9

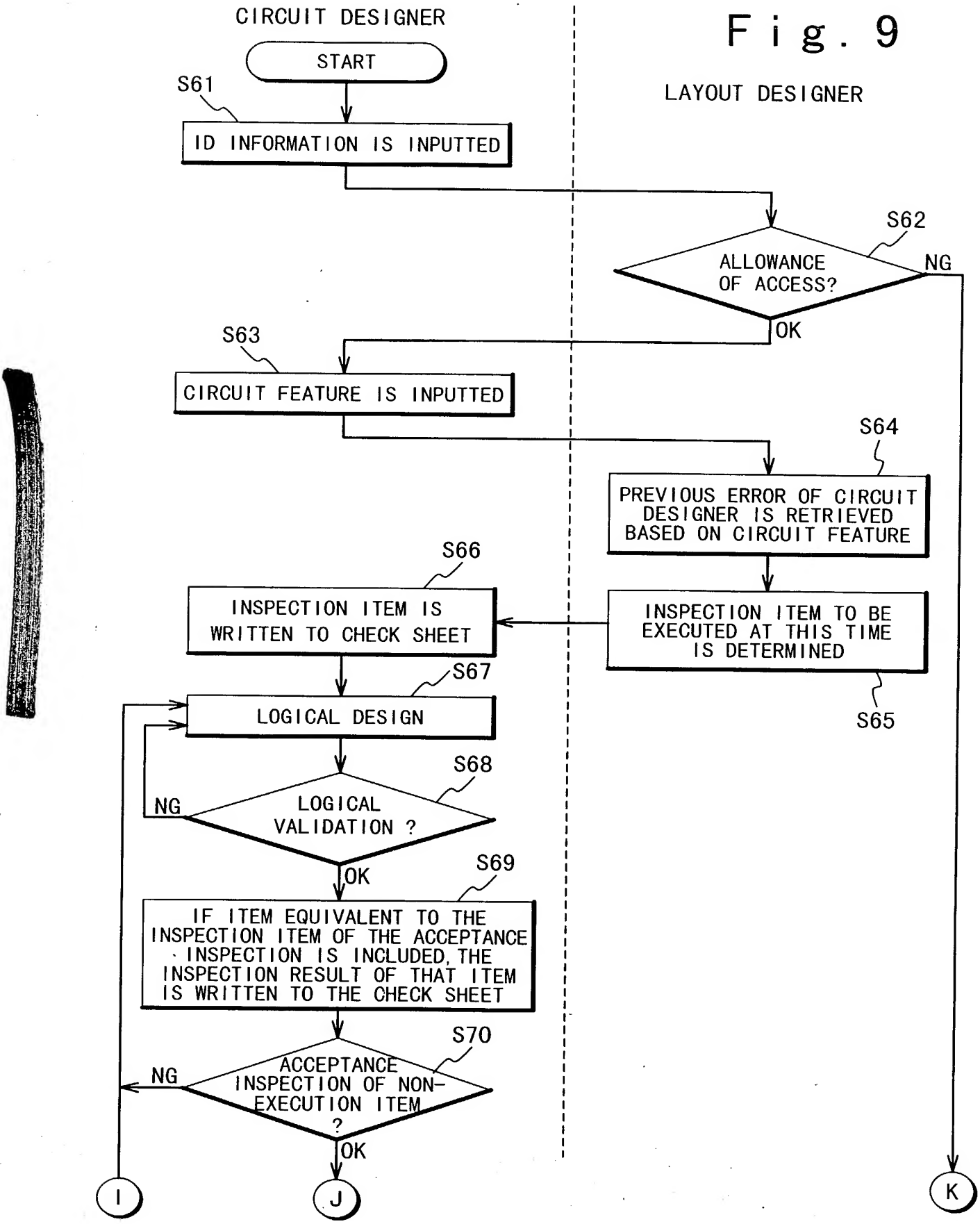

CIRCUIT DESIGNER
LAYOUT DESIGNER
START
S61
ID INFORMATION IS INPUTTED
S62
ALLOWANCE OF ACCESS?
NG
OK
S63
CIRCUIT FEATURE IS INPUTTED
S64
PREVIOUS ERROR OF CIRCUIT DESIGNER IS RETRIEVED BASED ON CIRCUIT FEATURE
INSPECTION ITEM TO BE EXECUTED AT THIS TIME IS DETERMINED
S65
S66
INSPECTION ITEM IS WRITTEN TO CHECK SHEET
S67
LOGICAL DESIGN
S68
LOGICAL VALIDATION ?
NG
OK
S69
IF ITEM EQUIVALENT TO THE INSPECTION ITEM OF THE ACCEPTANCE INSPECTION IS INCLUDED, THE INSPECTION RESULT OF THAT ITEM IS WRITTEN TO THE CHECK SHEET
S70
ACCEPTANCE INSPECTION OF NON-EXECUTION ITEM ?
NG
OK
I
J
K

Fig. 10

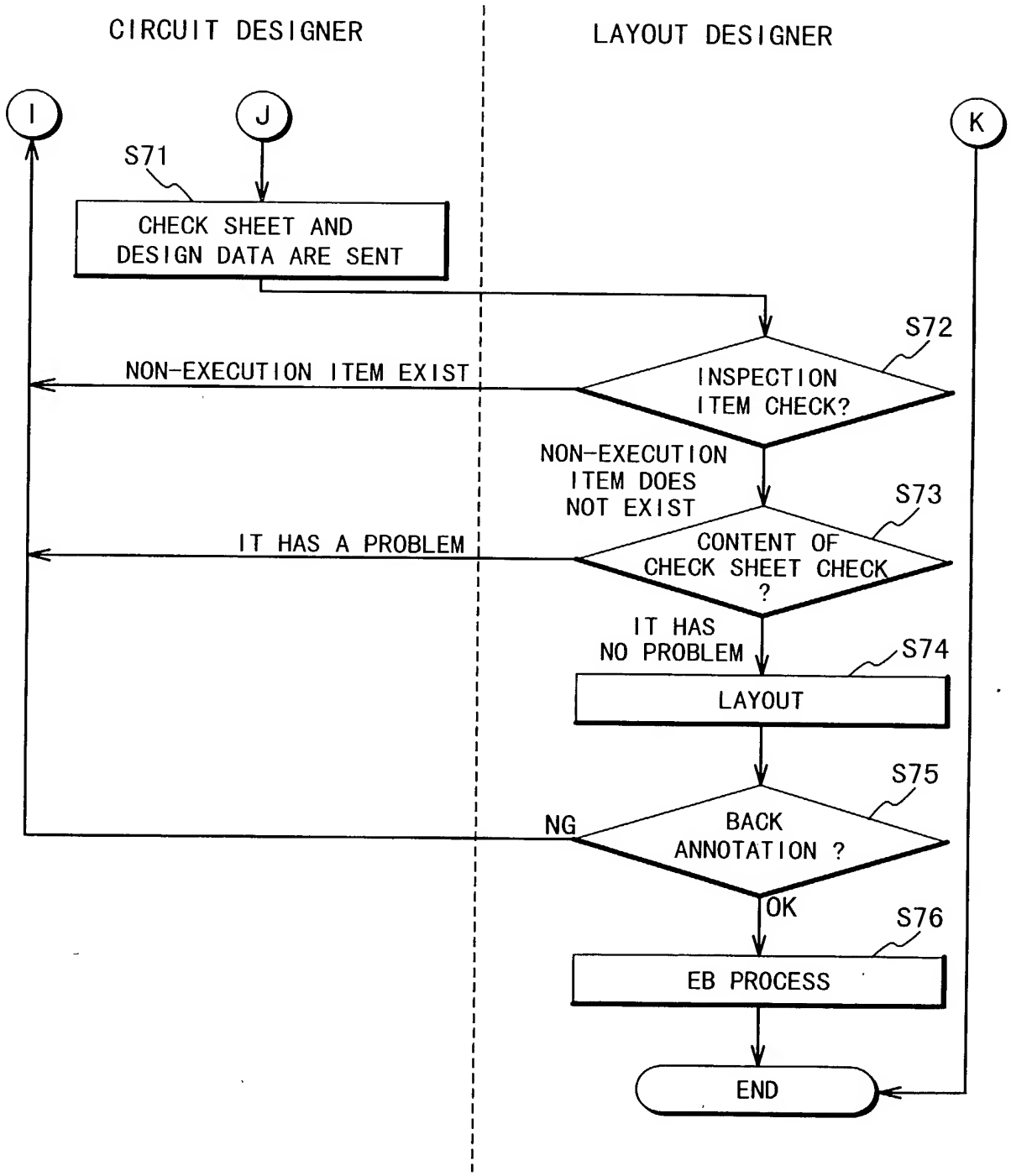

CIRCUIT DESIGNER
LAYOUT DESIGNER
I
J
K
S71
CHECK SHEET AND DESIGN DATA ARE SENT
S72
INSPECTION ITEM CHECK?
NON-EXECUTION ITEM EXIST
NON-EXECUTION ITEM DOES NOT EXIST
S73
CONTENT OF CHECK SHEET CHECK ?
IT HAS A PROBLEM
IT HAS NO PROBLEM
S74
LAYOUT
S75
BACK ANNOTATION ?
NG
OK
S76
EB PROCESS
END

Fig. 11

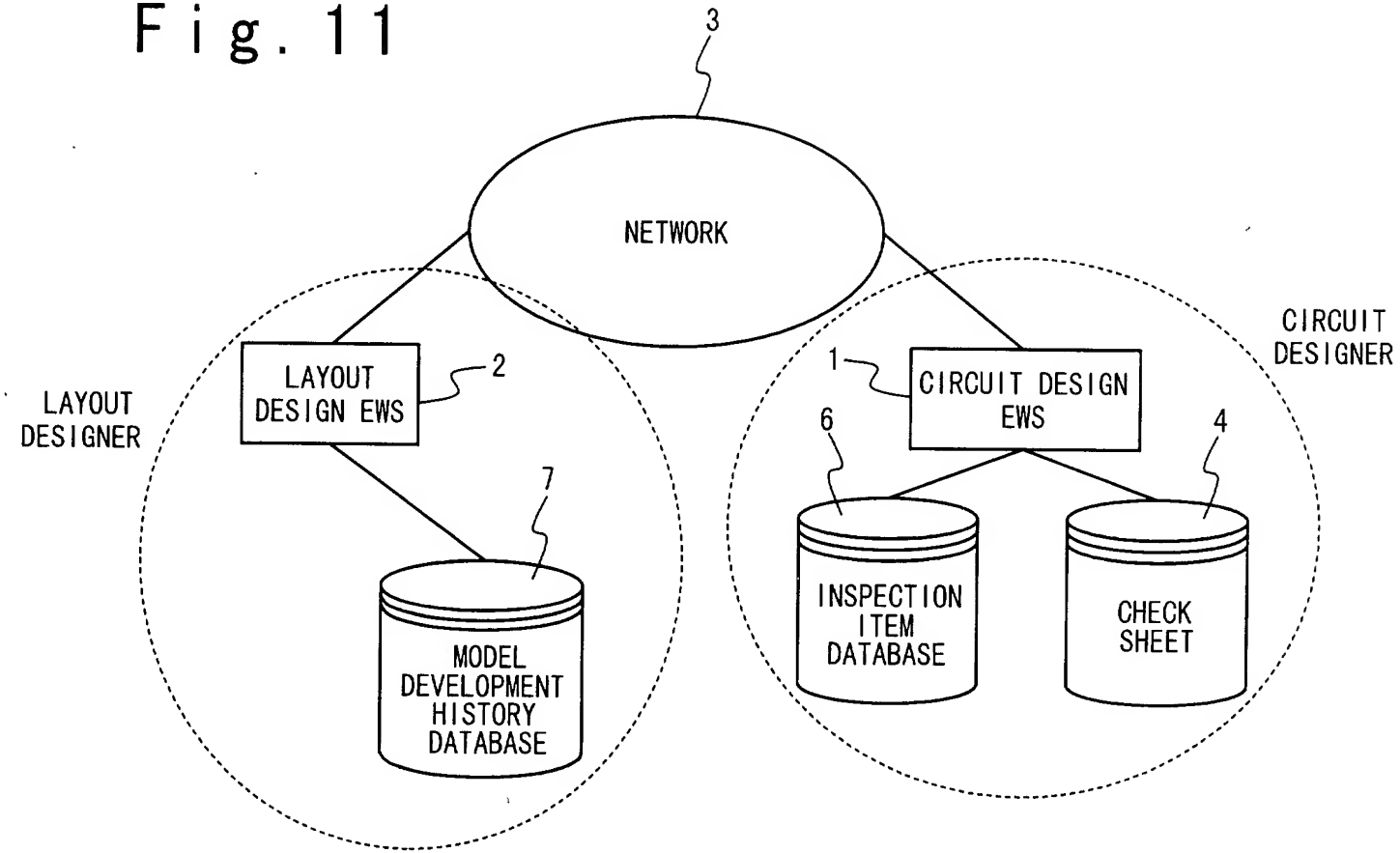

3
NETWORK
LAYOUT DESIGNER
LAYOUT DESIGN EWS
2
7
MODEL DEVELOPMENT HISTORY DATABASE
CIRCUIT DESIGNER
1
CIRCUIT DESIGN EWS
6
4
INSPECTION ITEM DATABASE
CHECK SHEET

Fig. 12

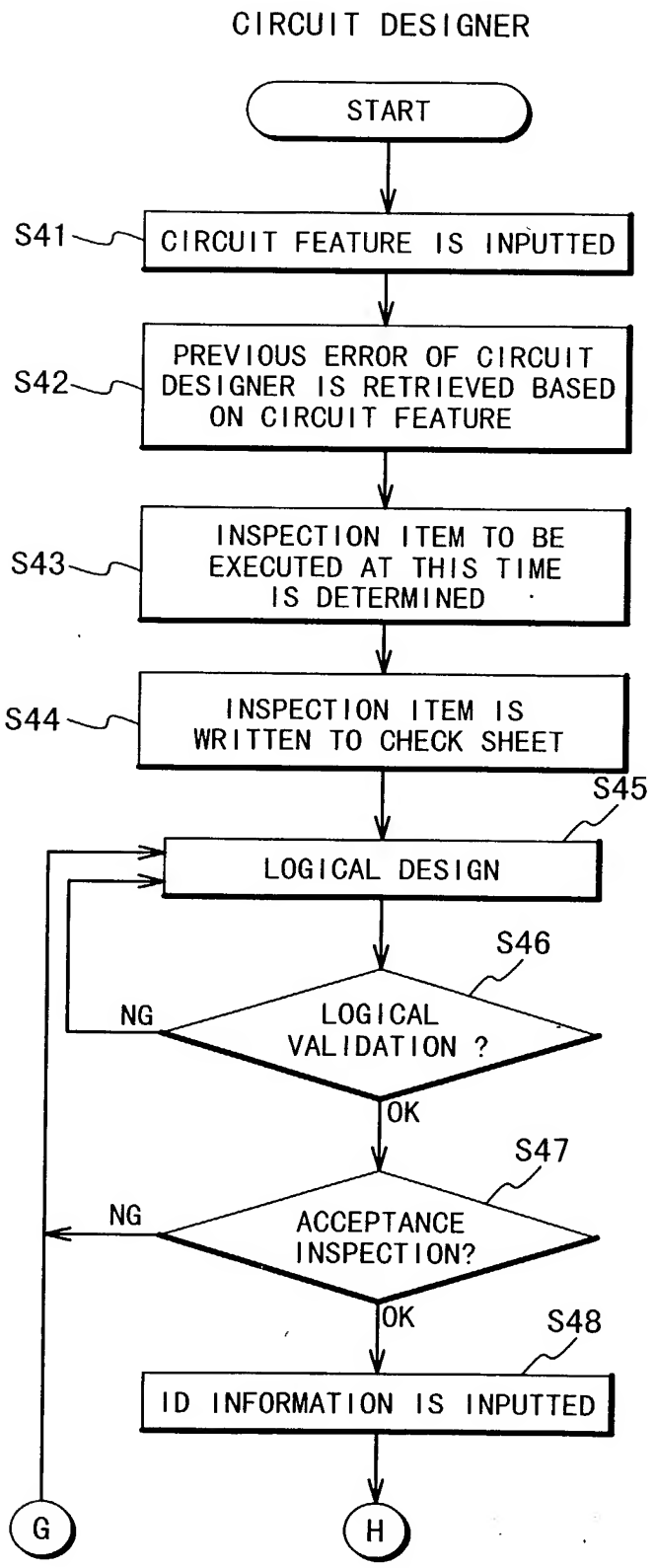

CIRCUIT DESIGNER
LAYOUT DESIGNER
START
S41
CIRCUIT FEATURE IS INPUTTED
S42
PREVIOUS ERROR OF CIRCUIT DESIGNER IS RETRIEVED BASED ON CIRCUIT FEATURE
S43
INSPECTION ITEM TO BE EXECUTED AT THIS TIME IS DETERMINED
S44
INSPECTION ITEM IS WRITTEN TO CHECK SHEET
S45
LOGICAL DESIGN
S46
NG
LOGICAL VALIDATION ?
OK
S47
NG
ACCEPTANCE INSPECTION?
OK
S48
ID INFORMATION IS INPUTTED
G
H

Fig. 13

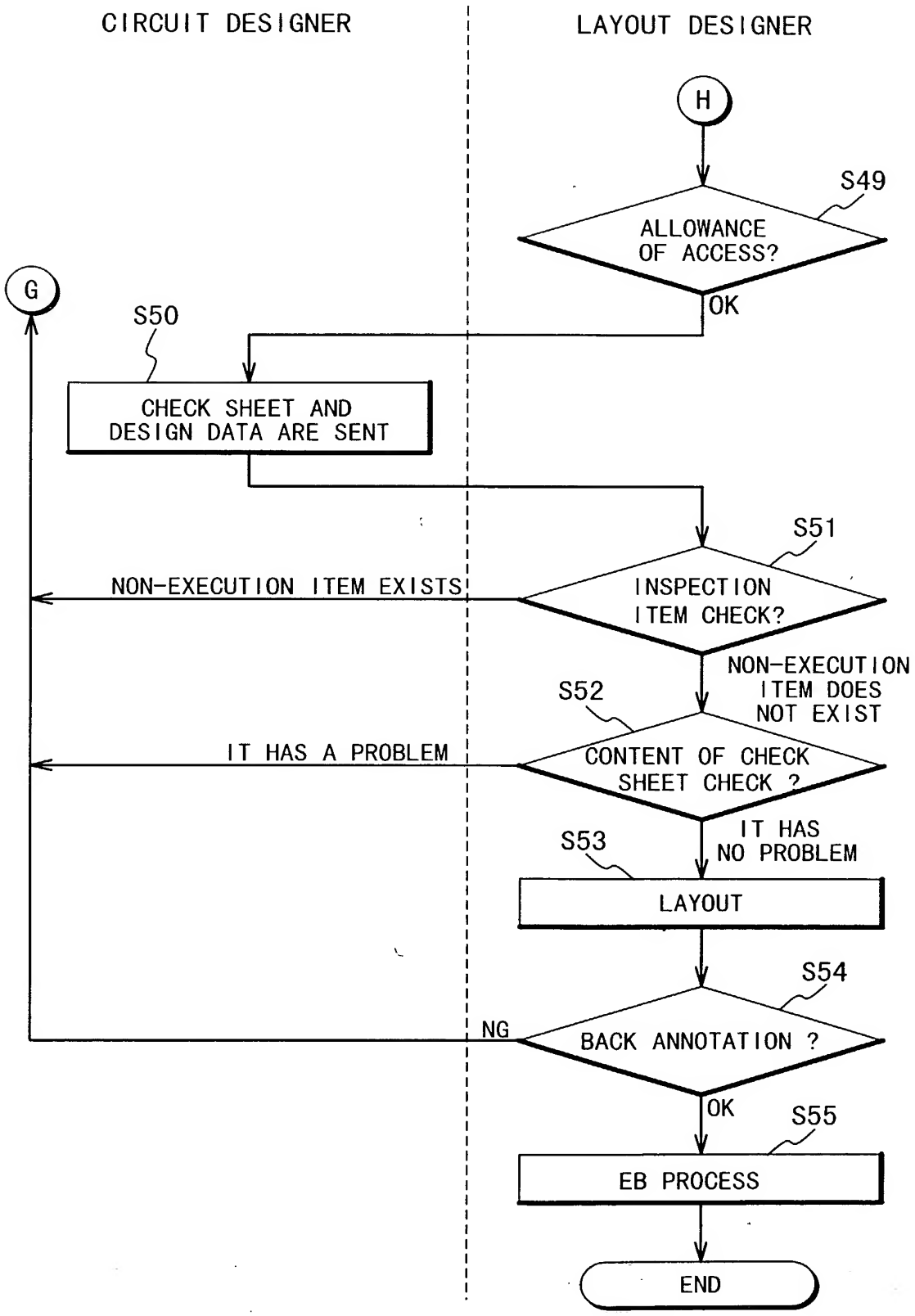
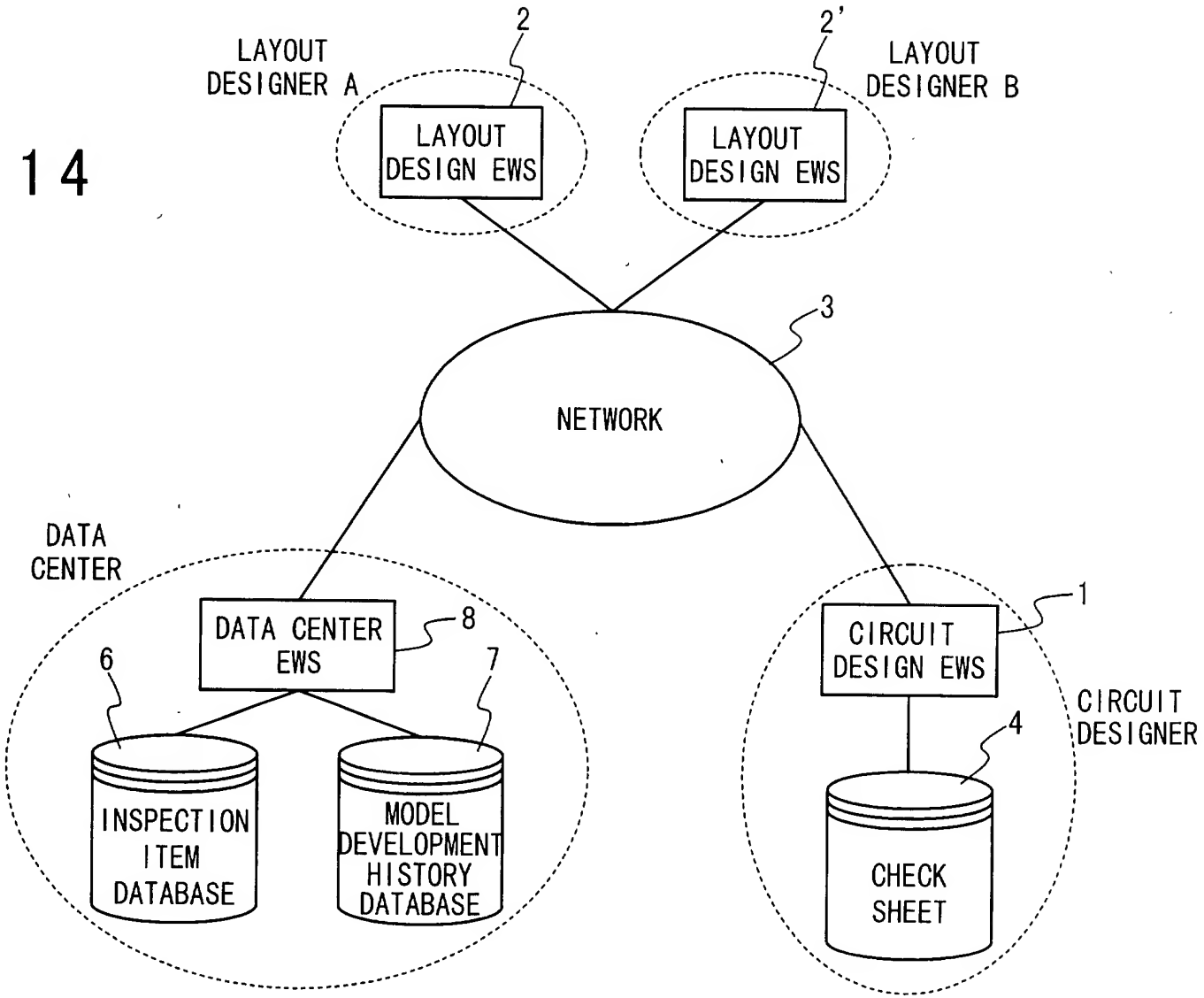

CIRCUIT DESIGNER
LAYOUT DESIGNER
H
S49
ALLOWANCE OF ACCESS?
OK
G
S50
CHECK SHEET AND DESIGN DATA ARE SENT
S51
NON-EXECUTION ITEM EXISTS
INSPECTION ITEM CHECK?
NON-EXECUTION ITEM DOES NOT EXIST
S52
IT HAS A PROBLEM
CONTENT OF CHECK SHEET CHECK ?
IT HAS NO PROBLEM
S53
LAYOUT
S54
NG
BACK ANNOTATION ?
OK
S55
EB PROCESS
END

Fig. 14


LAYOUT DESIGNER A
2
LAYOUT DESIGN EWS
2'
LAYOUT DESIGNER B
LAYOUT DESIGN EWS
3
NETWORK
DATA CENTER
DATA CENTER EWS
8
6
7
INSPECTION ITEM DATABASE
MODEL DEVELOPMENT HISTORY DATABASE
1
CIRCUIT DESIGN EWS
CIRCUIT DESIGNER
4
CHECK SHEET